Mobile Semiconductor

SPSRAMHS65LL - Single Port High Speed Memory C

Technology

SMIC

- 65nm Low Leakage
- Silicon Proven and production ready
- Silicon Test Report available
- Single Port SRAM with 6T Bitcell (0.525 sq µ)
- 700MHz Operation

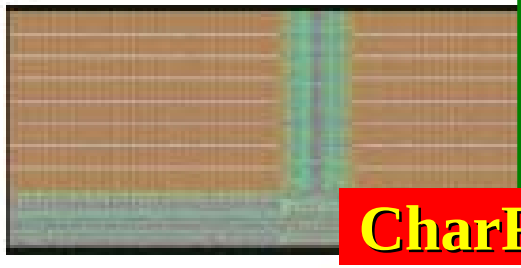
Key Features

- Max Instance: 80Kb
- Min Instance: 128b
- Operating Range:
  - 1.08V to 1.32V
  - -40C to +125C.
- 4 Metal Layers
- Power mesh architecture minimizes instance area
- Bit write
- Optional column redundancy
- Internal BIST Mux
- Functional, BIST and Scan test modes
- Compiler with GUI and Command Line Interface

Robust and production ready

Mobile Semiconductor's proprietary silicon prov
layout techniques have been applied to optimiz
keeping die size small. Low V_T and standard V_T
to optimize the critical path enhancing performa
static current.

In order to ensure high manufacturing yield, the
SPSRAMHS65LL utilizes standard SMIC 6T Bi
and is consistent with SMIC's Design For Manu
guidelines.



High quality and usability

Based on the production proven EMS[2] Trailblaze Compiler technology, SPSRAMHS65LL instances range from 128b to 80Kb at speeds up to 700MHz. All signal and power pins are available on M4 while maintaining over 50% routing porosity in M4. Aspect ratio and Bit Write capability are user configurable.

	Min	Max	Increment
Word Width	8	80	1
Word Depth	16	2048	2 * Column Fold

Design Views
GDS Layout including leaf cells
Spice Netlist for LVS
HCEL list of cells for LVS
LEF: P & R abstract
Behavioral Verilog
Liberty File
Verilog Test Bench
PDF and Text Datasheet
MemChar setup

CharFlo-Memory!

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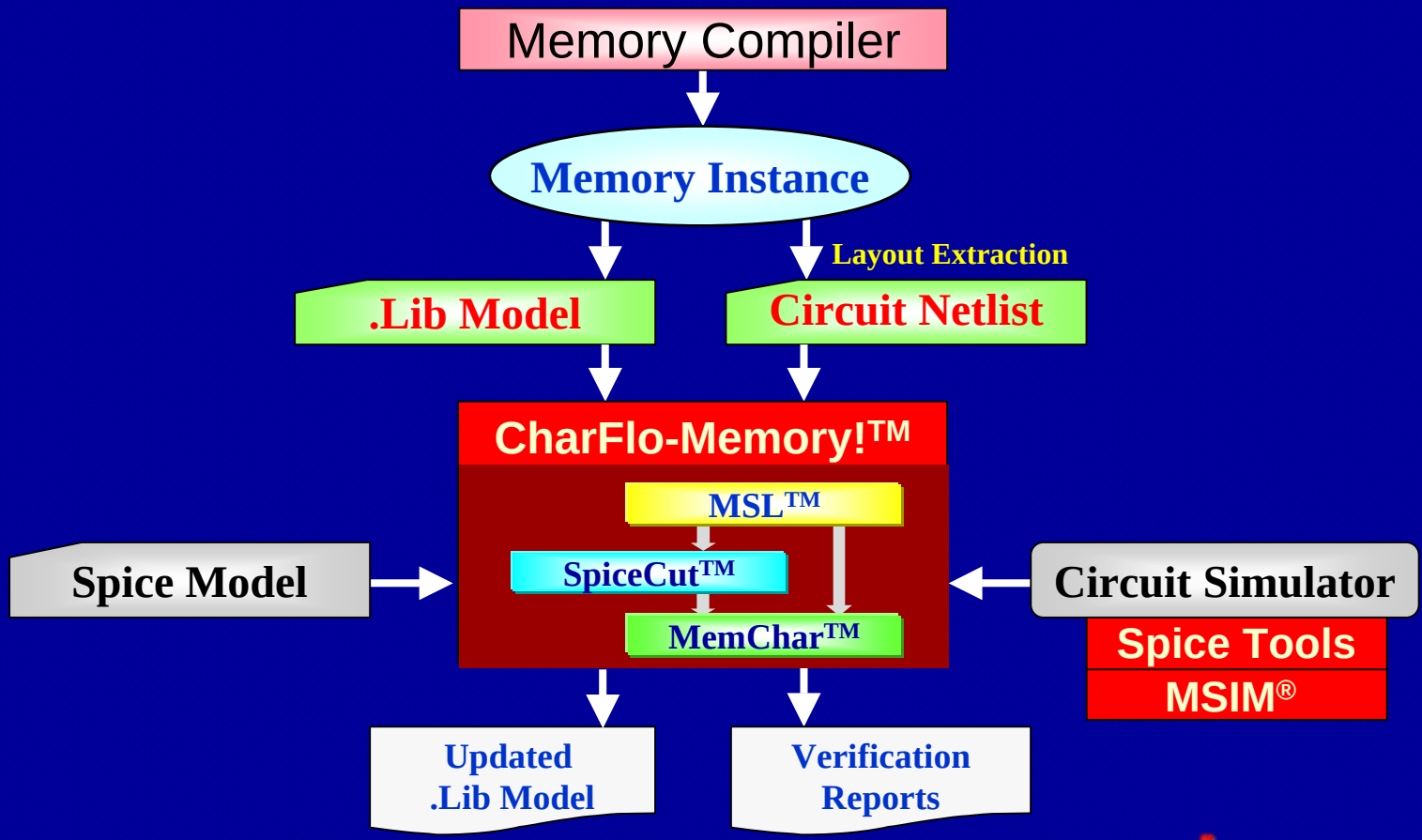
Legend Design Technology

Characterization Flow

For Compiled Memory Instances



The Features

Legend's CharFlo-Memory! Tool Set

- Production & silicon proven over numerous designs
- Perform "on-the-fly" verification for high reliability
- Build critical-path circuits from layout-extracted circuit for high performance
- Enable 'active-net' only layout extraction, RC reduction, and SPDM function for high productivity
- Support CCS timing, power and noise models
- Foundry and IP vendors' support
- Excellent price-performance and automation