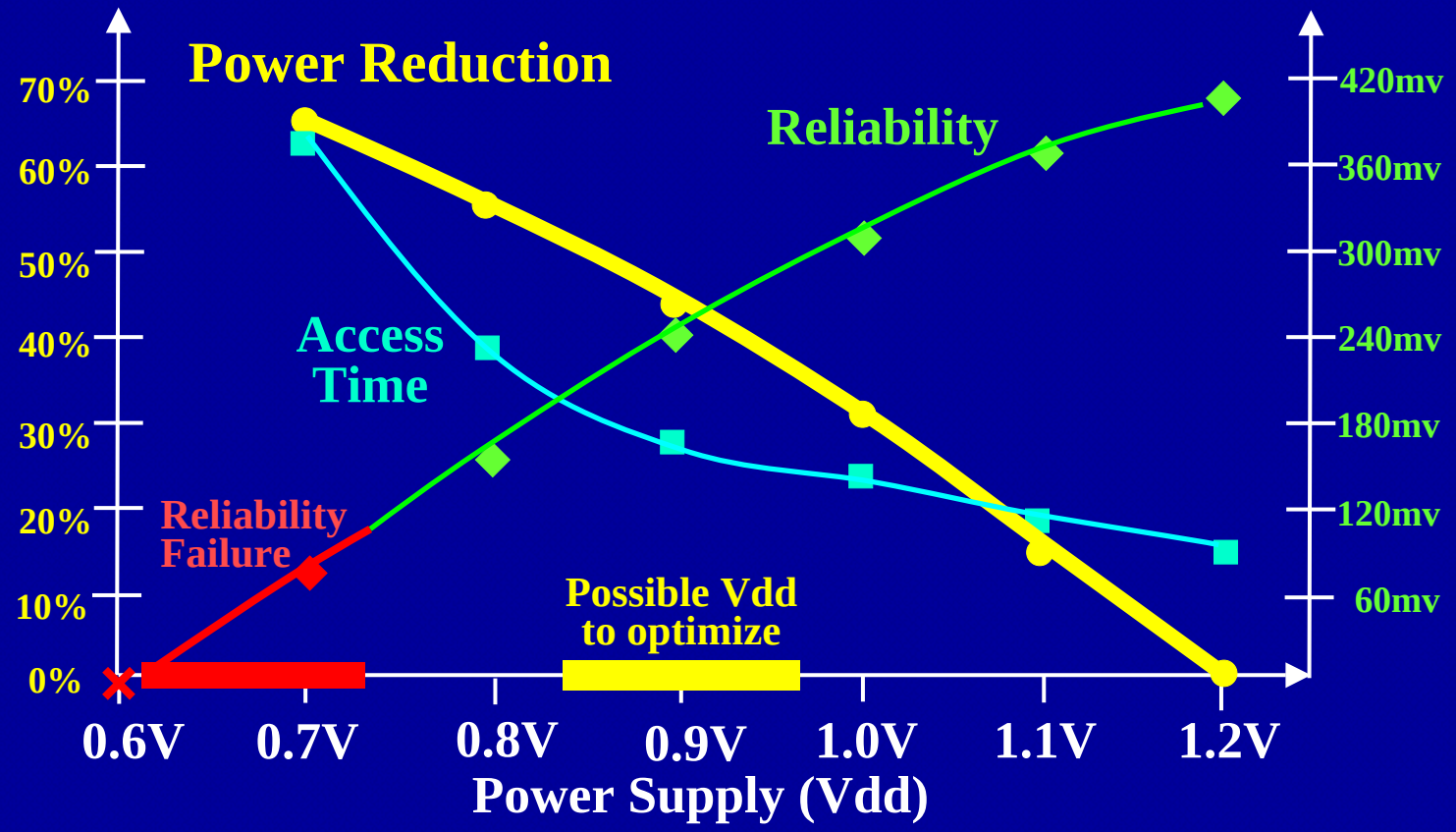
Power Supply Optimization

Power Reduction, Reliability & Performance



Power Supply Optimization

Memory Sense-Amp Signal vs Access Time

- Access time versus Sense-amp input signal at various power supply can be verified against noise margin.
- The power supply can be optimized for lower power.

Power Supply	Access Time	V(Bit, BitB)
1.2 V	1.66 ns	417 mV
1.1 V	1.92 ns	369 mV
1.0 V	2.30 ns	314 mV
0.9 V	2.89 ns	245 mV
0.8 V	3.98 ns	160 mV
0.7 V	6.40 ns	73.4 mV
0.6 V	FAIL	FAIL

** The voltage difference between Bit and BitB, V(Bit, BitB), need be over noise margin (e.g. 100 mV).*

Process and Analysis

Lowering Vdd to Reduce Chip's Power

- Determine Vdd by optimizing and balancing
  - Power reduction
  - Performance degrading
  - Reliability issues, and
  - Yield prediction and failure rate analysis
- Re-characterize those on-chip memories under that newly optimized low Vdd.
- Optimize read-margin setting under new Vdd